Operation of the HC55185 Ringing SLIC & IDT821054 Evaluation Module

Application Note | May 2002 | AN1003.1

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Functional Description

This application note is intended to supplement IDT's Evaluation Board User's Guide. The Users guide describes the Evaluation Board System and use of its software. The system includes one IDT821054 evaluation board, one HC55185 evaluation board and control software IDT821054.exe. For discussion purposes, the IDT821054 evaluation board will be referred to as the Mother Board and the HC55185 evaluation board will be referred to as the Daughter Board.

A good understanding of the material in the Users Guide is a prerequisite to this application note. For a detailed engineering analysis of the reference design using the HC55185 and IDT821054, see application note AN9998.

With this system, the user can configure a channel to channel conversation and perform various tests on the system using a Wandel and Golterman (W&G) PCM4.

The IDT821054 Evaluation Board System can be configured in two modes of operation via JP1, JP2 & JP3 on the mother board.

- **Emulation Mode,** Emulation Mode gets its name from the evaluation board's ability to emulate a far end callee (or caller) telephone conversation as a stand alone unit. In this mode the DC performance of the SLIC (logic state, Tip & Ring voltage levels, on hook & off hook detection) and channel to channel conversation is easily evaluated using the on-board clock circuit of the Mother Board.

  Jumper configuration:
  JP1 jumper IN (shorting DX/DR)
  JP2 jumper IN (providing power to the on board oscillator)
  JP3 IN (connecting INTERNAL clock to board)

- **Test Mode,** Test Mode gets its name from the evaluation board's ability to test the performance of the system using a PCM4. In this mode the AC performance of the half channel (D/A, A/D, D/D) can be evaluated.

Jumper configuration:
JP1 jumper OUT
JP2 jumper OUT
JP3 IN (connecting EXTERNAL clock to board)

This application note will first evaluate the DC performance of the system by configuring the Jumpers in the Emulation Mode. Figure 3 shows the required connection between the Evaluation Board, PC, PCM4 tester and Power Supplies. Proper connection should be established before running the software.

If the user prefers to evaluate the AC performance first, then along with the proper connections (Figure 3) and jumpers positioned for the test mode, the user needs to insure the clock of the PCM4 is connected before running the software.

Verifying Basic Operation

The operation of the Mother & Daughter Boards can be verified by performing the following tests:

1. Normal Loop Feed Verification
   Tip & Ring Voltage Forward Active State, On Hook
   Tip & Ring Voltage Forward Active State, Off Hook
   Tip & Ring Voltage Reverse Active State, On Hook
   Tip & Ring Voltage Reverse Active State, Off Hook
2. Loop Supervisory Detection
   On Hook & Off Hook
   Tip Open State, Ground Key Test
   Forward Loopback State
3. Ringing Verification
4. Programming of Coefficients
5. Emulation of Far End Telephone Conversation
6. Gain Verification
   Total System Gain (Digital to Digital)
7. Variable Gain/Frequency
   Receive Gain (Digital to Analog)
   Transmit Gain (Analog to Digital)
8. Total Distortion
   Receive Gain (Digital to Analog)
   Transmit Gain (Analog to Digital)

HC55185 Daughter Board

The HC55185EVAL1 evaluation board is optimized to match either a 600Ω or a 200Ω + 680Ω||0.1μF line impedances, have a Ring Trip Threshold of 76mA, a Switch Hook Threshold of 12mA, Loop Current Limit of 24.6mA and a Transient Current Limit of 95mA.

The daughter board is a dual channel board that enables testing between adjacent channels (CH1 to CH2, CH3 to CH4, CH5 to CH6, and CH7 to CH8). An additional daughter board can be obtained to enable testing between all channels. Reference the application note AN9998 for calculation of external components and programming coefficients.

Programming of the logic state of the SLIC, loop supervisory detection, time slot allocation, coefficients, tone/ teletax signals are all controlled via software using the MPI screen (Figure 2).

IDT821054 Mother Board

The IDT821054 Mother Board provides a way to evaluate the operation of IDT's IDT821054 and Intersil's HC55185 Ringing SLIC. The programming interface illustrated in this application note is the Microprocessor Interface (MPI). Figure 1 shows the IDT821054 mother board component locations. The location of jumpers JP1, JP2, and JP3 are highlighted with arrows. JP1 is used to short the DX and DR

signals from the PCM4 to prevent interference when Emulation Mode testing is performed. JP2 connects power to the on-board clock. This enables setup of the software without having to use the clock from the PCM4. JP3 connects either the on-board clock or the clock from the PCM4. Proper operation of the software requires this clock signal.

Getting Started

The following steps will configure the Mother Board for testing in either the Emulation Mode or the Test Mode.

1. Connect IDT821054, HC55185 and PCM4 as shown in Figure 3. Note: The Daughter Board gets its power from the Mother Board.
2. Set the General Parameters of the PCM4 as shown in Table 2 (see Test #6).
3. Once power is applied and the appropriate clock is supplied to the Mother Board (i.e. internal clock for Emulation Mode, or PCM4 clock for Test Mode), PRESS the reset button. The LED will flash and then remain on. This will synchronize the clock and enable software control from the PC.
4. Initialize the software by clicking on IDT821054.exe and select the desired Operating Mode (MPI), COM Port and SLIC from the Mode and Port selection screen then click OK.
5. The MPI Mode screen will then appear (Figure 2). All programming of the channels and monitoring of SLIC status are performed using this screen.
6. From MPI Software screen, select Channel 1 in the left shaded area.
7. From MPI Software screen, select Global operation in the left shaded area. Accept defaults or set to your preferences and click the Write button.
8. From MPI Software screen, click on the Auto Detect Enable box. This will enable the CODEC to detect the status of the SLIC. Detection will be in the form of the receiver next to the channel indicator, left shaded area, being one of the 4 indicators located at the bottom of the shaded area in the Legend (Active, Ring, In Use, Power Off). The Auto Detect Enable box will also activate the I/O Pin Status of the SLICs $\overline{\text{DET}}$ pin via SI1. A red color signifies a logic one and green color a logic zero.
9. From MPI Software screen, clicking on the Broadcast Mode will enable the user to configure multi-channels at the same time.
10. From MPI Software screen, Select: Active F, BSEL L, Power On and click the Write button. **The SLIC is now ready to be tested.**

Test # 1 Normal Loop Feed Verification

This test verifies the correct tip and ring voltages in both onhook and offhook forward active and reverse active states. Loop current and ground key detect are also verified via the software MPI screen.

Discussion

The HC55185 is designed to have its most positive 2-wire terminal (tip in the forward active state and ring in the reverse active state) fixed at a set voltage. The most negative 2-wire terminal voltage is dependent upon the load across tip and ring and the programmable current limit.

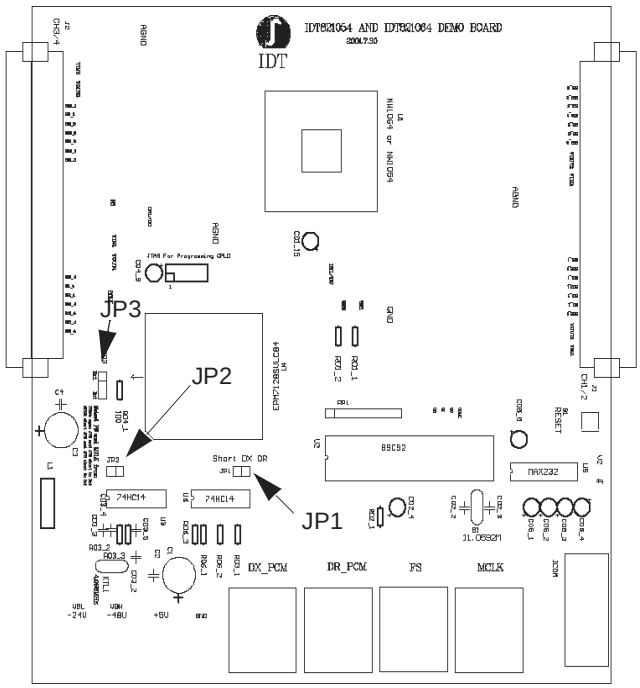


FIGURE 1. IDT821054 MOTHER BOARD COMPONENT LOCATION

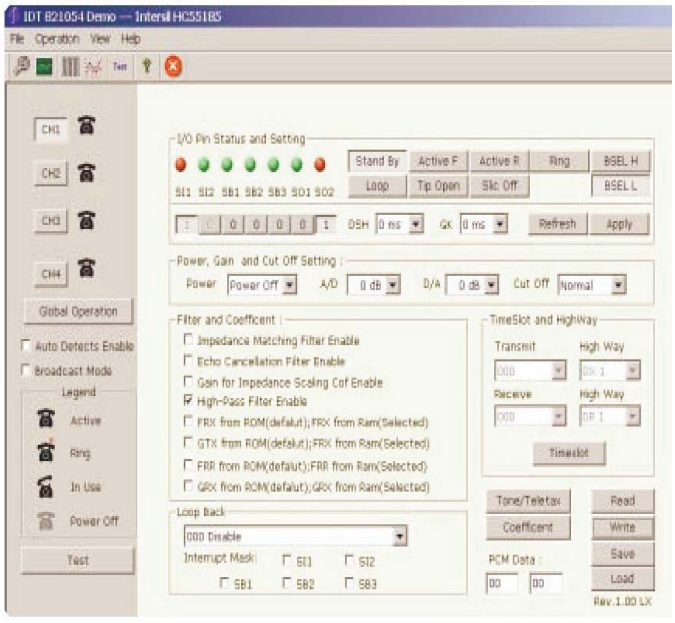


FIGURE 2. MPI OPERATION GENERAL INTERFACE

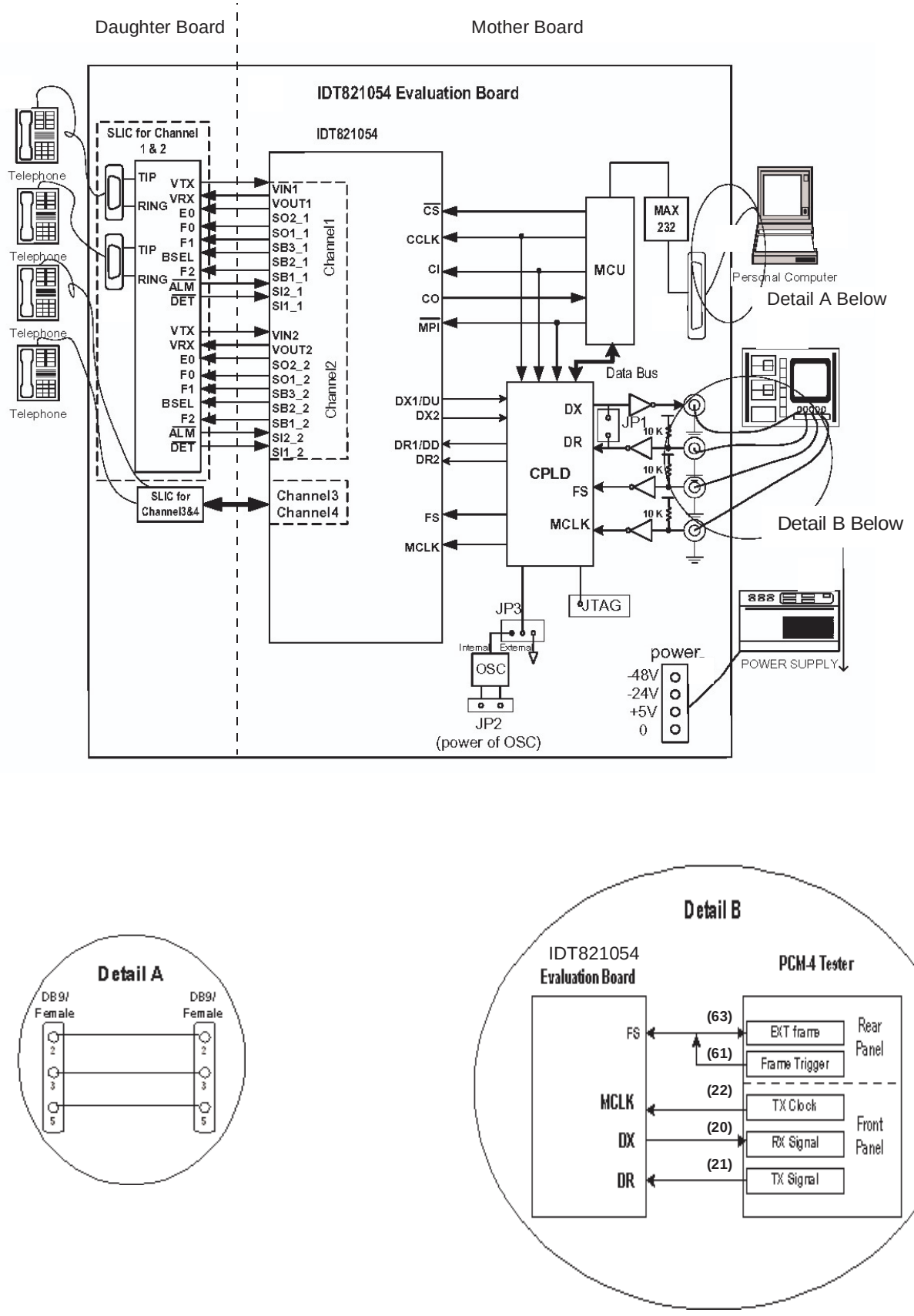


FIGURE 3. IDT821054 MOTHER BOARD CONNECTIONS

Loop supervision is provided by either the switch hook or the ground key detectors. Loop status is observed by monitoring the I/O Pin SI1 of the MPI screen. The device may be operated from either high or low battery for on-hook transmission, during ringing and low battery for loop feed.

When operating from the high battery, the DC voltages at Tip and Ring are MTU compliant. The typical Tip voltage is -4V and the Ring voltage is a function of the battery voltage for battery voltages less than -60V as shown in Equation 1.

$$V_{RING} = V_{BH} + 4 \quad \text{(EQ. 1)}$$

Most applications will operate the device from low battery while off hook. The DC feed characteristic of the device will drive Tip and Ring towards half battery to regulate the DC loop current. For light loads, Tip will be near -4V and Ring will be near V_{BL} + 4V. Figure 4 shows the DC feed characteristic.

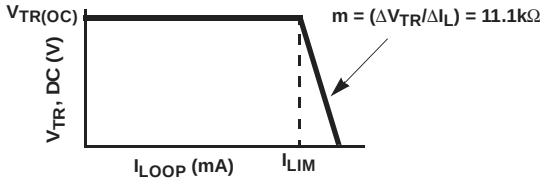


FIGURE 4. DC FEED CHARACTERISTIC

The point on the y-axis labeled $V_{TR(OC)}$ is the open circuit Tip to Ring voltage and is defined by the feed battery voltage.

$$V_{TR(OC)} = |V_{BL}| - 8 \quad \text{(EQ. 2)}$$

The Ground Key detector operation is verified by configuring the HC55185 in the tip open state and grounding the ring pin. Grounding the ring pin results in a current that triggers an internal detector that pulls the output of $\overline{DET}$ low causing I/O Pin SI1 to turn Green.

The Forward Loop Back mode provides test capability for the device. An internal signal path is enabled allowing for both DC and AC verification. The internal 600Ω terminating resistor has a tolerance of ±20%. The device is intended to operate from only the low battery during this mode.

When the forward loop back mode is initiated internal switches connect a 600Ω load across the outputs of the Tip and Ring amplifiers as shown in Figure 5.

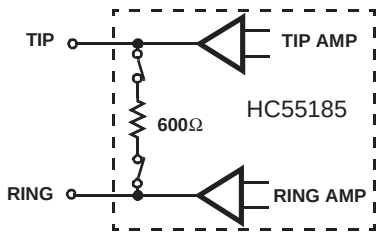


FIGURE 5. FORWARD LOOP BACK INTERNAL TERMINATION

When the internal signal path is provided, DC current will flow from Tip to Ring. The DC current will force $\overline{DET}$ low causing I/O Pin SI1 to turn Green.

Measuring Tip and Ring Voltages

1. Configure Hardware and Software as described in section titled" Getting Started".
2. Configure Mother Board for Emulation Mode. Verify:
   - Jumper JP1 is IN,
   - JP2 is IN,
   - JP3 is set to Internal BCLK.

NOTE: Once the software is initiated (section "Getting Started"), the user can switch between Emulation and Test modes and still maintain software control.

3. From MPI Software screen, Select: Active F, BSEL H, Power On and click the Write button.
4. Measure the tip and ring voltages (reference Figure 6) and compare to those in Table 1 (onhook).
5. Terminate TIP and RING with a 600Ω load via the RJ11 jack.
6. Measure tip and ring voltages with respect to ground and compare to those in Table 1 (offhook 600Ω).
7. From MPI Software screen, Select: Active R, BSEL H, Power On and click the Write button.
8. Disconnect the 600Ω load from across tip and ring.
9. Repeat steps 4, 5, 6 and 8.

TABLE 1. TIP AND RING VOLTAGES

LOGIC STATE	R_L (Ω)	TIP VOLTAGE REFERENCEDT O GND	RING VOLTAGE REFERENCED TO GND
Forward Active V_{BH} = -48V V_{BL} = NA V_{CC} = +5V	Onhook	-3.6 — -4.6	-37.0 — -44.0
	Offhook 600Ω	-13.5 — -17.0	-28.0 — -32.0
Reverse Active V_{BH} = -48V V_{BL} = NA V_{CC} = +5V	Onhook	-38.0 — -44	-3.5 — -4.5
	Offhook 600Ω	-28.0 — -32.0	-13.5 — -17.0

Test # 2 Loop Supervisory Detection

Verification of Switch Hook Detect

If previous test was Test #1, skip to step 3.

1. Configure Hardware and Software as described in section titled" Getting Started".
2. Configure Mother Board for Emulation Mode. Verify:
   - Jumper JP1 is IN,
   - JP2 is IN,
   - JP3 is set to Internal BCLK.

NOTE: Once the software is initiated (section "Getting Started"), the user can switch between Emulation and Test modes and still maintain software control.

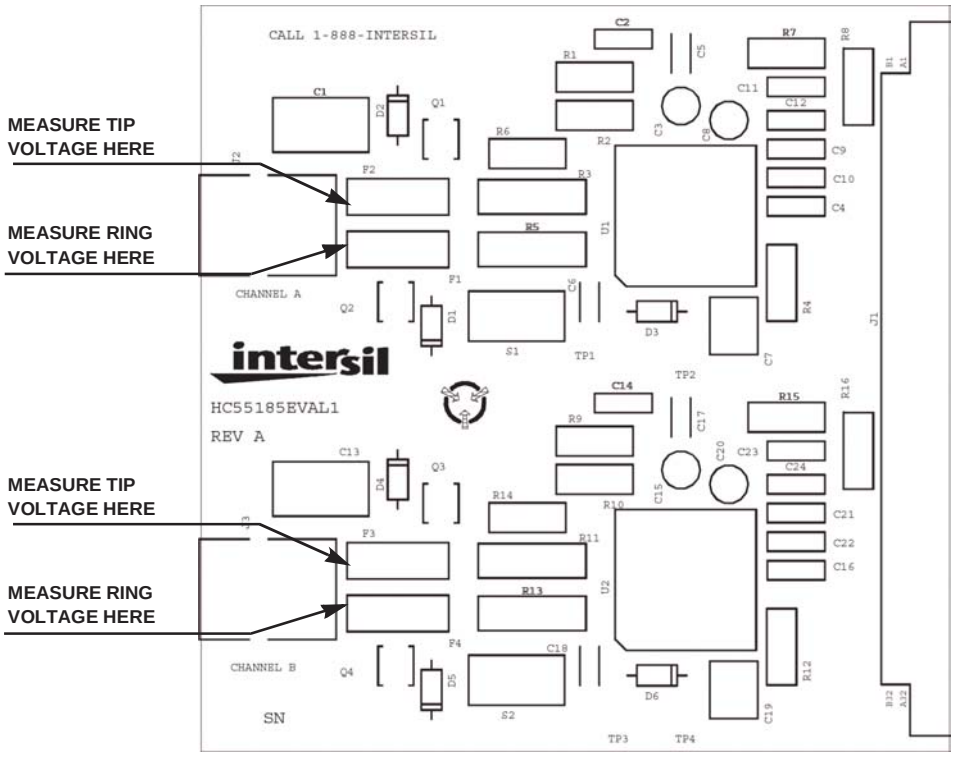


FIGURE 6. DAUGHTER BOARD LAYOUT

3. With the SLIC in either the forward active state (Active F) or reverse active state (Active R), the phone icon (left shaded area of the MPI screen) indicates In Use and the I/O Pin SI1 turns Green when tip and ring are terminated with 600Ω and Active and Red respectively when tip and ring are an open circuit.

Verification of Ground Key Detect

1. From MPI Software screen, Select: Tip Open, BSEL H, Power On and click the Write button.
2. The phone icon (left shaded area of the MPI screen) indicates Active and the I/O Pin SI1 is Red.
3. Grounding the ring terminal will verify Ground Key Detect when the phone icon (left shaded area of the MPI screen) indicates In Use and the I/O Pin SI1 turns Green.

Verification of Forward Loopback

1. From MPI Software screen, Select: Loop, BSEL L, Power On and click the Write button.
2. Verification of Forward Loopback operation is when the phone icon (left shaded area of the MPI screen) indicates In Use and the I/O Pin SI1 is Green.

Test # 3 Ringing Verification

This test will demonstrate the ability of the IDT821054 to ring a phone through the HC55185. A telephone is the only additional hardware required to complete this test.

Discussion

The HC55185 provides linear amplification to support a variety of ringing waveforms. A programmable ring trip function provides loop supervision and auto disconnect upon ring trip. The device is designed to operate from the high battery during this mode.

Architecture

The device provides linear amplification to the signal applied to the ringing input, V_{RS}. The differential ringing gain of the device is 80V/V. The circuit model for the ringing path is shown in Figure 7.

The voltage gain from the VRS input to the Tip output is 40V/V. The resistor ratio provides a gain of 8 and the current mirror provides a gain of 5. The voltage gain from the VRS input to the Ring output is -40V/V. The equations for the Tip and Ring outputs during ringing are given in Equations 3 and 4.

$$V_T = \frac{V_{BH}}{2} + (40 \times VRS) \quad \text{(EQ. 3)}$$

$$V_R = \frac{V_{BH}}{2} - (40 \times VRS) \quad \text{(EQ. 4)}$$

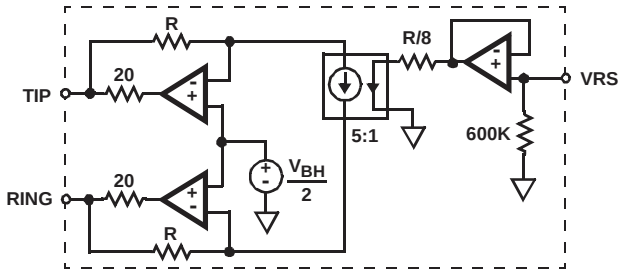


FIGURE 7. LINEAR RINGING MODEL

When the input signal at VRS is zero, the Tip and Ring amplifier outputs are centered at half battery. The device provides auto centering for easy implementation of sinusoidal ringing waveforms. Both AC and DC control of the Tip and Ring outputs are available during ringing. This feature allows for DC offsets as part of the ringing waveform.

Ringing Input

The ringing input, V_{RS}, is a high impedance input. The high impedance allows the use of low value capacitors for AC coupling the ring signal. The V_{RS} input is enabled only during the ringing mode, therefore a free running oscillator may be connected to VRS at all times.

When operating from a battery of -100V, each amplifier, Tip and Ring, will swing a maximum of $95V_{P-P}$. Hence, the maximum signal swing at VRS to achieve full scale ringing is approximately $2.4V_{P-P}$. The low signal levels are compatible with the output voltage range of the CODEC. The digital nature of the CODEC ideally suits it for the function of programmable ringing generator.

Ringing the Phone

If previous test was either Test #1 or #2, skip to step 3.

1. Configure Hardware and Software as described in section titled" Getting Started".
2. Configure Mother Board for Emulation Mode. Verify:
   - Jumper JP1 is IN,
   - JP2 is IN,
   - JP3 is set to Internal BCLK.

NOTE: Once the software is initiated (section "Getting Started"), the user can switch between Emulation and Test modes and still maintain software control.

3. From MPI Software screen, Select: CH 1, Active F, BSEL H, Power On and click the Write button.
4. From MPI Software screen, Select: Tone/Teletax. The Dual Tone and Teletax Setting screen will appear. Under Dual Tone Setting select:
   Frequency: Tone 2 = 20, Tone 1= 20
   Tone 2 = Enable
   Tone 1 = Enable
   Tone 2 Gain = 1, Tone 1 Gain = 1.
   Then click the Write button.
5. Connect a phone to Channel 1 using the RJ11 jack on the Daughter Board
6. Set VBH supply to -100V.
7. From MPI Software screen, Select Ring and the phone will start to ring. Cadencing of the ring signal is accomplished by switching between Ring and Active F (or Active R). Note: the command to the SLIC is immediate, you don't have to press Write for the command to be invoked.
8. When the test is completed, you need to Disable the 2 Tones. This will prevent the tone from interfering with subsequent tests.
9. Set VBH supply back to -48V.

Test # 4 Programming of Coefficients

Using the DSP coefficients provided by IDT, the overall performance of the system will pass ITU-T requirements.

When the COF RAM button is selected from the MPI Operation General Interface screen, the COF RAM Operation screen will appear (Figure 8). From this screen, the user can load the coefficients for the current channel.

For IDT to calculate IDT821054 DSP coefficient, customers should provide the following information about their subscriber line card:

- Accurate SLIC PSPICE model. It can be provided in .lib file or PSPICE schematic file.
- System Impedance
- Gain (Transmit path and Receive path)

IDT will then provide the user with 4 files, one for each channel. An example of a file name is: HC55185_600_1. The first portion of the file name is the SLIC being used (HC55185). The second portion of the file name is the line impedance the coefficients are matching (600Ω) and the last portion is the channel (1).

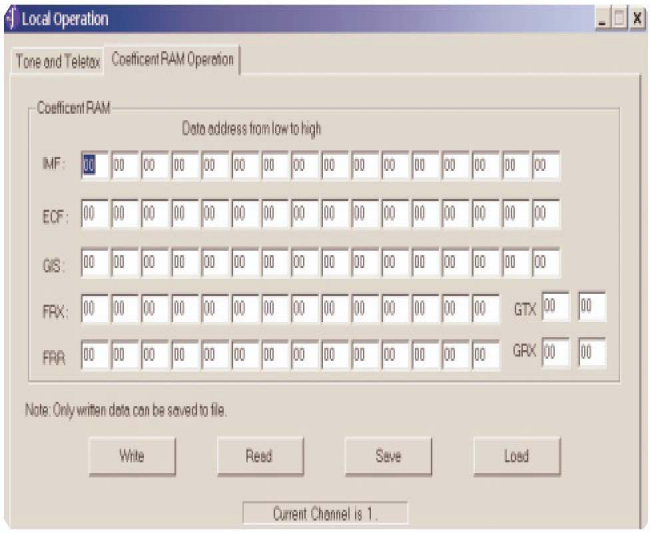


FIGURE 8. COEFFICIENT RAM OPERATION SCREEN

Loading Coefficients

If previous test was Test #1, #2 or #3, skip to step 3.

1. Configure Hardware and Software as described in section titled" Getting Started".
2. Configure Mother Board for Emulation Mode. Verify:
   - Jumper JP1 is IN,
   - JP2 is IN,
   - JP3 is set to Internal BCLK.

NOTE: Once the software is initiated (section "Getting Started"), the user can switch between Emulation and Test modes and still maintain software control.

3. From MPI Software screen, Select the desired Channel by clicking on the channel button in the left shaded area
4. From MPI Software screen, Select COF RAM**.** The Coefficient Ram Operation screen will appear (Figure 8).

   Down loading Coefficients from a File:

   - Click on Load and the desk top window opens. Navigate to where the file is stored and select the coefficients for the channel being programmed. Opening the file will automatically load the coefficients into COF RAM screen. Another window will appear to inform you that the file successfully loaded.
   - Click OK. Exit the screen by click the Close button (don't write files from this screen). This will return you to the MPI Software screen. Click Write from this screen.
5. Repeat steps 3 and 4 to load the coefficients for the other channels.

Test # 5 Emulation of Phone Conversation

This test will demonstrate an end to end phone conversation between Channel 1 and Channel 2. Setting up an end to end phone conversation is accomplished with the Timeslot and PCM Highway Assignment screen (Figure 9). The user can select any time slot for Channels transmit and receive. If the time slot assigned to the receive path of Channel X is the same one assigned to the transmit path of Channel Y, and the time slot assigned to the transmit path of Channel X is the same one assigned to the receive path of Channel Y, then Channel X and Channel Y can communicate with each other.

Assigning Timeslots

If previous test was Test #1, #2, #3 or #4, skip to step 3.

1. Configure Hardware and Software as described in section titled" Getting Started"
2. Configure Mother Board for Emulation Mode. Verify:
   - Jumper JP1 is IN,
   - JP2 is IN,
   - JP3 is set to Internal BCLK.

NOTE: Once the software is initiated (section "Getting Started"), the user can switch between Emulation and Test modes and still maintain software control.

3. From MPI Software screen, Select Tone and Teletax Settings and verify that both the Tones are Disabled. This will prevent the tone signals from interfering with the Channel to Channel communication.
4. From MPI Software screen, Select Timeslot. The Timeslot and PCM Highway Assignment screen will appear (Figure 9).
5. For communications between Channel 1 and Channel 2, one possible configuration is:

   Set Channel 1 Transmit = 000, DX1
   Set Channel 1 Receive = 001,DR1
   Set Channel 2 Transmit = 001,DX1
   Set Channel 2 Receive = 000, DR1
6. Set the transmit and receive paths as shown in step 5 and click the Write button.
7. Connect Phones to the RJ11 jacks of both Channels 1 and Channel 2. Communication between Channels 1 and 2 is now possible.

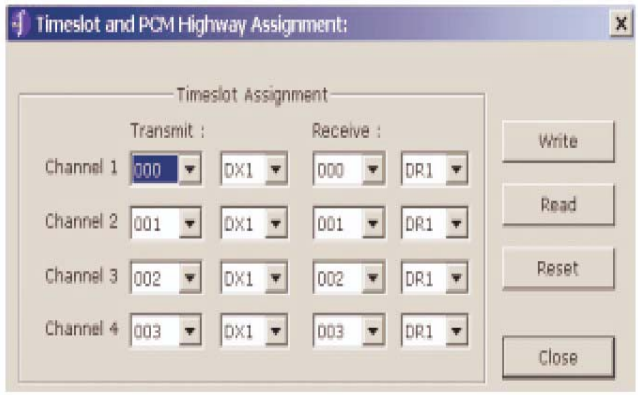


FIGURE 9. TIMESLOT & PCM HIGHWAY ASSIGNMENT SCREEN

Test # 6 Gain Verification

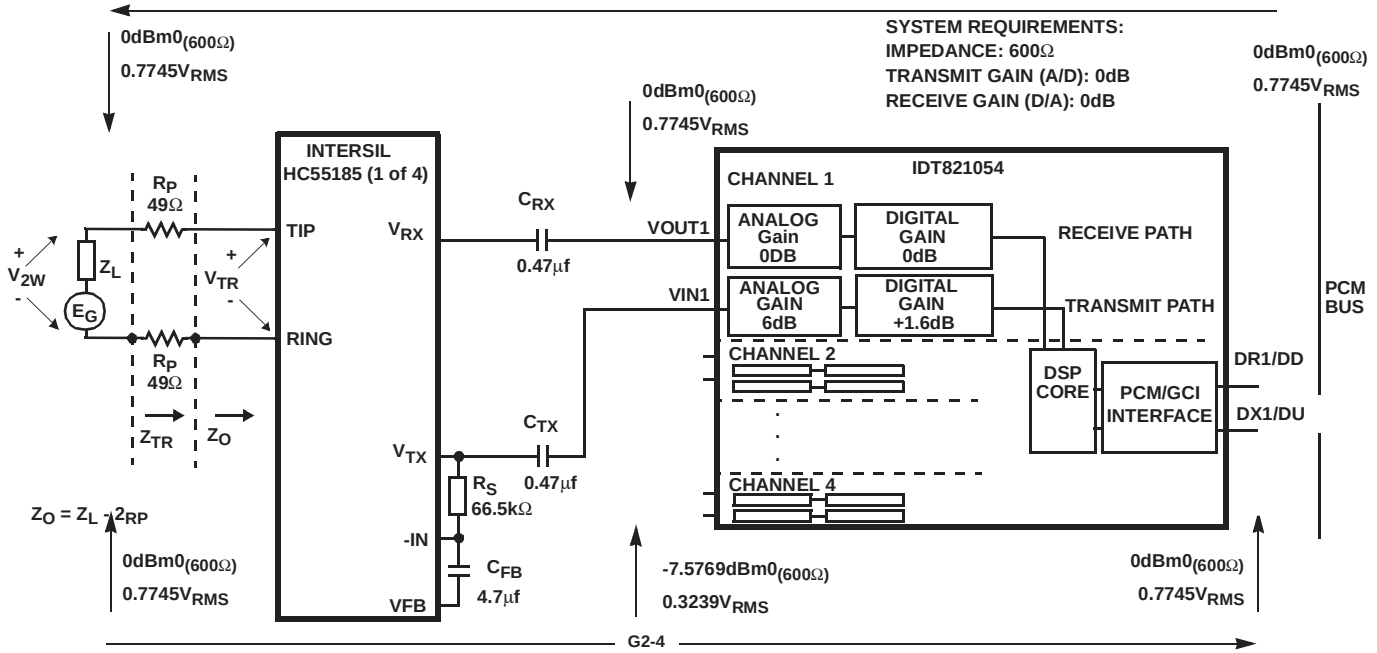
This test will verify the gains through the IDT821054 and the HC55185 are operating properly. The test will show, with the proper coefficients loaded into the CODEC, the Digital to Analog gain across both the CODEC and the SLIC is equal to -1.0 (0.0dB), and the Analog to Digital gain across both the SLIC and the CODEC are also equal to 1.0 (odB). Both D/A and A/D gains will be verified by performing a Digital to Digital gain using the PCM4.

Figure 10 shows the reference design of the HC55185 and the IDT821054 with a 600Ω load impedance and transmit and receive gains of 0dB. Reference An9998 for a detailed engineering analysis of the reference design.

Total System Gain (D/D)

If previous test was Test #1, #2, #3, #4 or #5, skip to step 2.

1. Configure Hardware and Software as described in section titled" Getting Started"
2. Prerequisite for this test is that test #4 "Programming of Coefficients" be completed using the 600Ω coefficients, system gains: (A/D = 0dB, D/A = 0dB) and CODEC analog gains: (A/D = +6dB, D/A = 0dB) Table 1 of application note AN9998.
3. Terminate tip and ring with a 600Ω load via the RJ11 jack.



NOTE: Reference Table 1 **AN9998** for coefficients.

FIGURE 10. REFERENCE DESIGN OF THE HC55185 AND THE IDT821054 WITH A 600Ω LOAD IMPEDANCE

4. Configure Mother Board for TEST Mode. Verify:

- Jumper JP1 is OUT,
- JP2 is OUT,
- JP3 is set to External BCLK.

   Note: Once the software is initiated (section “Getting Started”), the user can switch between Emulation and Test modes and still maintain software control.

5. Set the General Parameters of the PCM4 as shown in Table 2.
6. Set the PCM4 transmit and receive channels to channel 0. This will enable the PCM4 to receive and transmit data to the Channel 1 PCM time slot. To test channel 2 of the Mother Board, set the PCM4 to channel 1. Continue this pattern for remaining channels.
7. From MPI Software screen, set the A/D (Transmit) Gain = +6dB and the D/A (Receive) Gain = 0dB.
8. Configure the PCM4 for the MODE A 11 test. Set PCM4 to D-D, SWP/S (single sweep). Press start to test network.

Verification

Compare results to the Figure11

TABLE 2. PCM4 GEN. PARAMETERS SETTINGS

GENERAL PARAMETER	SETTING	PARM
(1) Digital Configuration:		
General configuration	TX/RX 2M/2Mbits/s selected	11
Digital Loop (A - A)	OPEN/AUX.SIGN.	23
(2) Frame Selection:		
TX frame type	All 32 TS teleph	14
RX frame type	All 32 TS teleph	24
CRC-4 Multiframe	Off	31

TABLE 2. PCM4 GEN. PARAMETERS SETTINGS (Continued)

GENERAL PARAMETER	SETTING	PARM
(3) Digital TX Interface:		
Line Code	NRZ	13
Output Impedance	75 ohms unbalanced	22
Clock	Int. 2048 kHz	31
(4) Digital RX I nterface:		
Line Code	NRZ	13
Input Impedance	> 3K Ohms	22
(5) Digital Words in TX Frame:	Reset to standard values	11
Frame Words	ALL CHAN.	22
Send Signal		
(6) TX Error Insertion	Off	11
(7) PCM Coding:		
TX Encoding Law	Must match switch S7-6 on IDT821054 EVM. Default setting on EVM is A-law	11
RX Encoding Law	Must match encoding law	21
(8) Scanner Parameter:		
VF-Input no.	1	11
VF-Output no.	1	21
(9) Special Parameter:		
Level Display	dBm0	11
Two wire Term.	Infinite	13
Digital Channel no.	Time Slot	16
	Mark and cont.	22
Tolerance mask set 2		23
	Mark and cont.	27
Clock display	OFF	33
OFF		35

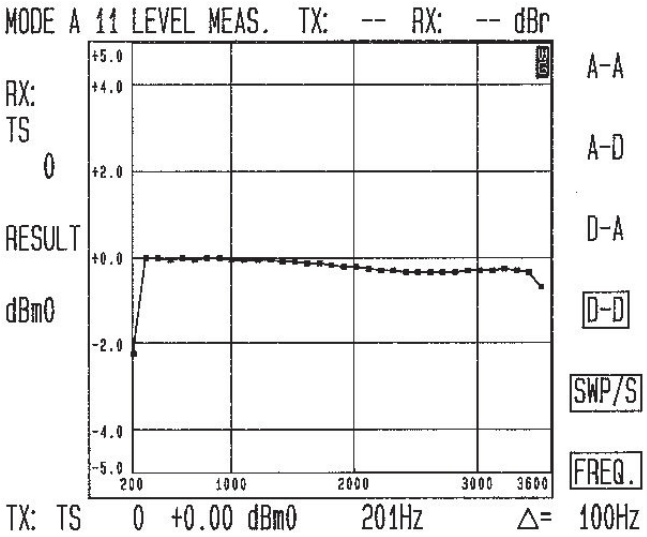


FIGURE 11. TOTAL SYSTEM GAIN (D/D)

Test # 7 Variation of Gain / Frequency

This test will configure the HC55185 in the loopback mode and evaluate the IDT821054 and the HC55185's AC performance across frequency.

Discussion

Most of the SLICs in the HC55185 family feature 2-Wire loopback testing. During the 2-wire loopback test, a 600Ω internal resistor is switched across the tip and ring terminals of the SLIC. This allows the DET function and the 4-wire to 4-wire AC transmission, right up to the subscriber loop, to be tested.

Variable Gain / Frequency (D/A) Test #7a

If previous test was Test #1, #2, #3, #4, or #5, skip to step 2. If previous test was Test # 6 skip to step 7.

1. Configure Hardware and Software as described in section titled" Getting Started"
2. Prerequisite for this test is that test #4 "Programming of Coefficients" be completed using the 600Ω coefficients, system gains: (A/D = 0dB, D/A = 0dB) and CODEC analog gains: (A/D = +6dB, D/A = 0dB) Table 1 of application note AN9947.
3. Configure Mother Board for TEST Mode. Verify:
   - Jumper JP1 is OUT,
   - JP2 is OUT,
   - JP3 is set to External BCLK.

NOTE: Once the software is initiated (section "Getting Started"), the user can switch between Emulation and Test modes and still maintain software control.

4. Set the General Parameters of the PCM4 as shown in Table 2.
5. Set the PCM4 transmit and receive channels to channel 0. This will enable the PCM4 to receive and transmit data to the Channel 1 PCM time slot. To test channel 2 of the Mother Board, set the PCM4 to channel 1. Continue this pattern for remaining channels.
6. From MPI Software screen, set the A/D (Transmit) Gain = +6dB and the D/A 9Receive Gain) = 0dB.
7. Remove the 600Ω load from across tip and ring.
8. From MPI Software screen, Select Loop
9. Configure the PCM4 for the MODE A 33 test. Set PCM4 to D-A, SWP/S (single sweep). Press start to test network.

Verification

Compare results to the Figure 12.

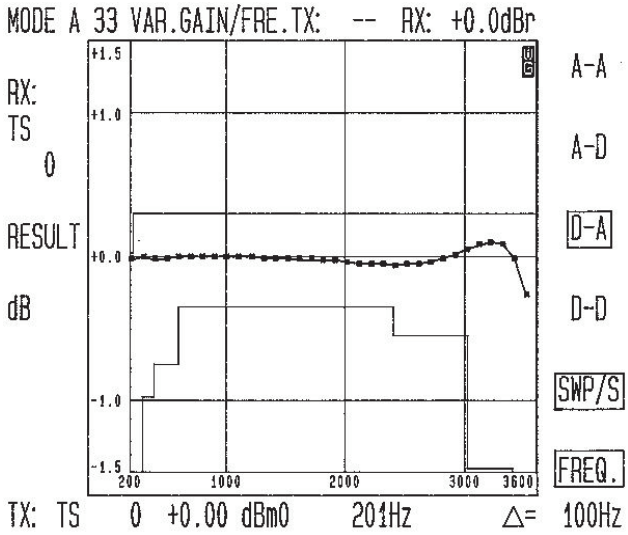


FIGURE 12. (D/A) VARIABLE GAIN vs. FREQUENCY

Variable Gain / Frequency (A/D) Test #7b

1. Configure the PCM4 for the MODE A 33 test. Set PCM4 to A-D, SWP/S (single sweep). Press start to test network.

Verification

Compare results to the Figure 13.

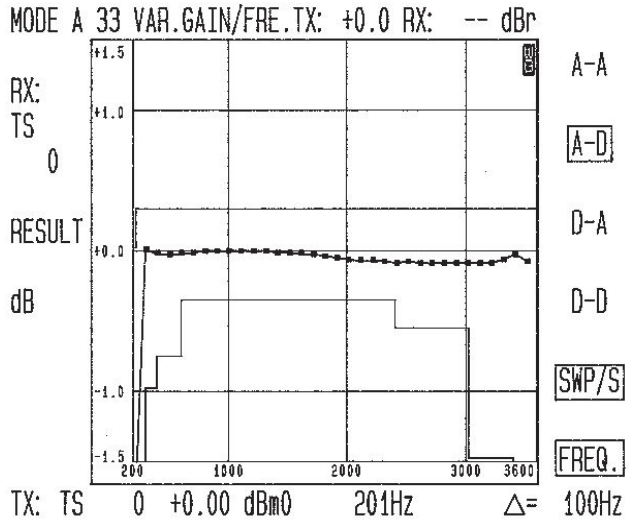


FIGURE 13. (A/D) VARIABLE GAIN vs. FREQUENCY

Test # 8 Total Distortion

This test will configure the HC55185 in the loopback mode and evaluate the IDT821054 and the HC55185's Total Distortion.

Total Distortion (D/A) Test #8a

If previous test was Test # 1, #2, #3, #4, or #5, skip to step 2.
If previous test was Test # 6 skip to step 7.
If previous test was Test #7a/b skip to step 9.

1. Configure Hardware and Software as described in section titled" Getting Started"
2. Prerequisite for this test is that test #4 "Programming of Coefficients" be completed using the 600Ω coefficients, system gains: (A/D = 0dB, D/A = 0dB) and CODEC analog gains: (A/D = +6dB, D/A = 0dB) Table 1 of application note AN9947.
3. Configure Mother Board for TEST Mode. Verify:
   - Jumper JP1 is OUT,
   - JP2 is OUT,
   - JP3 is set to External BCLK.

NOTE: Once the software is initiated (section "Getting Started"), the user can switch between Emulation and Test modes and still maintain software control.

4. Set the General Parameters of the PCM4 as shown in Table 2.
5. Set the PCM4 transmit and receive channels to channel 0. This will enable the PCM4 to receive and transmit data to the Channel 1 PCM time slot. To test channel 2 of the Mother Board, set the PCM4 to channel 1. Continue this pattern for remaining channels.
6. From MPI Software screen, set the A/D (Transmit) Gain = +6dB and the D/A 9Receive Gain) = 0dB.
7. Remove the 600Ω load from across tip and ring.
8. From MPI Software screen, Select Loop
9. Configure the PCM4 for the MODE A 55 test. Set PCM4 to D-A, SWP/S (single sweep). Press start to test network.

Verification

Compare results to the Figure 14.

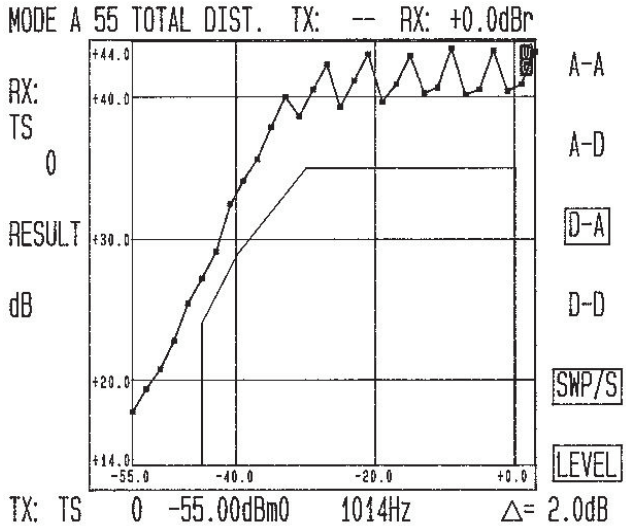


FIGURE 14. (D/A) TOTAL DISTORTION

Total Distortion (A/D) Test #8b

1. Configure the PCM4 for the MODE A 55 test. Set PCM4 to A-D, SWP/S (single sweep). Press start to test network.

Verification

Compare results to the Figure 15.

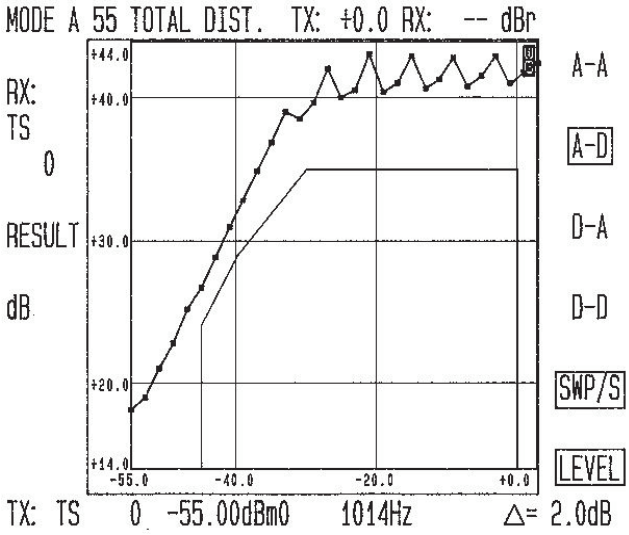


FIGURE 15. (A/D) TOTAL DISTORTION

Daughter Board Schematic

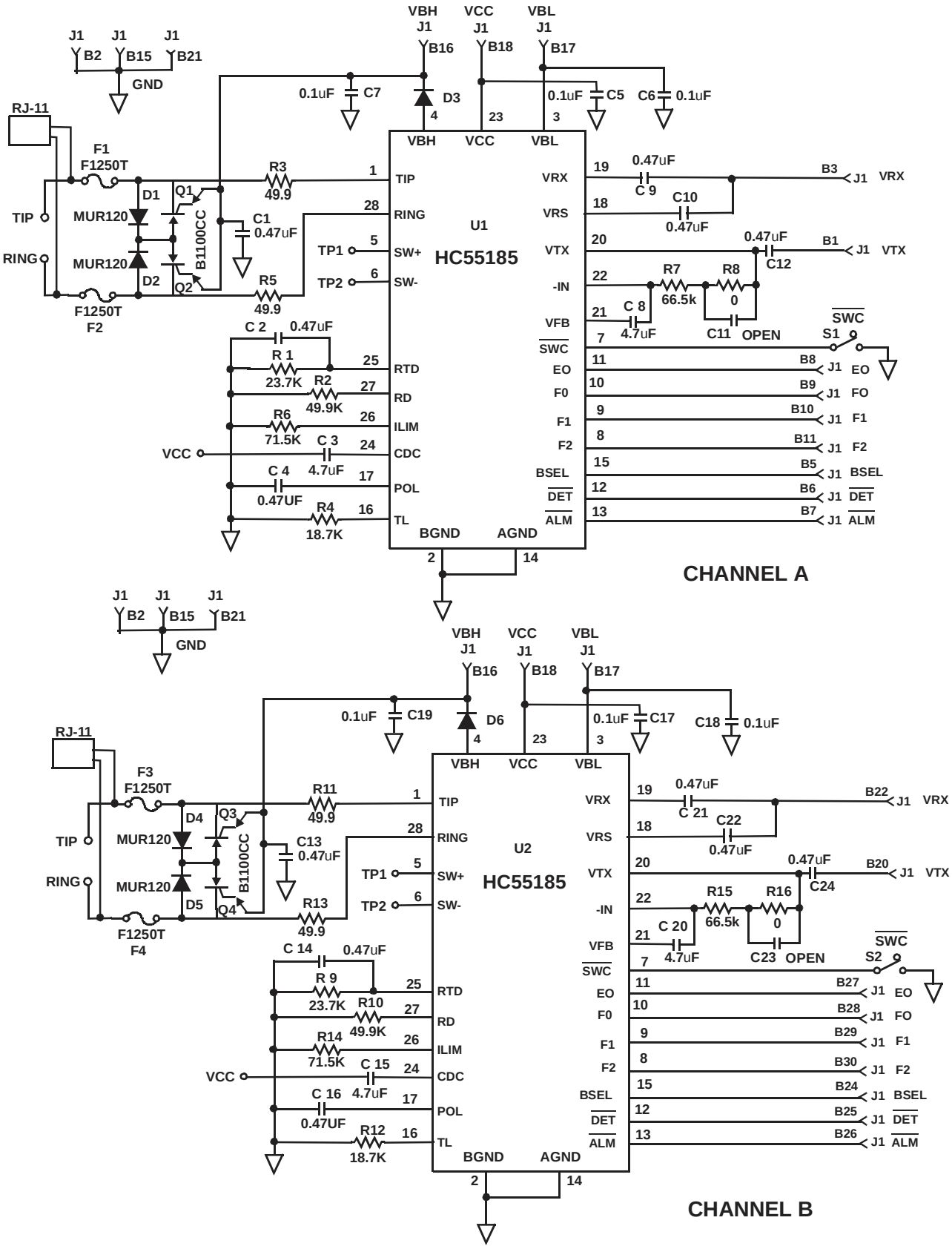


FIGURE 16. HC55185 DEMO DAUGHTER BOARD SCHEMATIC

TABLE 3. DAUGHTER BOARD COMPONENT LIST

COMPONENT	VALUE	TOLERANCE	RATING
U1,U2 - SLIC	HC55185	N/A	N/A
Q1,Q2,Q3,Q4 BATTRIX	B1100CC	N/A	N/A
R3, R5, R11, R13 (Line feed resistors)	49.9Ω	Matched 1%	2.0W
R1,R9	23.7kΩ	1%	1/16W
R2,R10	49.9KΩ	1%	1/16W
R4,R12	18.7kΩ	1%	1/16W
R6,R14	71.5kΩ	1%	1/16W
R7R15	66.5kΩ	1%	1/16W
R8,R16	0Ω	1%	1/16W
C2,C4,C9,C10,C12,C14,C16,C21,C22,C24	0.47µF	20%	50V
C1,C13	0.47µF	20%	200V
C3,C8,C15,C20	4.7µF	10%	50V
C5,C6,C17,C18	0.1µF	20%	50V
C7,C19	0.1µF	20%	200V
C11,C23	OPEN		
$\overline{DET}$ and $\overline{ALM}$ LEDs	Red	-	-
D1,D2,D4,D5	MUR120		
F1,F2,F3,F4	F1250T		
D3,D6, Recommended if the V_{BL} supply is not derived from the V_{BH} supply.	1N4004	-	-

Design Parameters: Ring Trip Threshold = 76mApeak, Switch Hook Threshold = 12mA, Loop Current Limit = 24.6mA, Transient current limit = 95mA.